Interconnects and Transitions in Multilayer LTCC Multichip Modules for 24 GHz ISM-Band Applications

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ABSTRACT

Multilayer LTCC substrates with screen printed conductors are considered as a key technology for coming RF wireless communication and automotive applications. Small but expensive MMICs should be integrated in a much cheaper LTCC environment to become a multichip module (MCM). Interconnects between the environmental waveguides and the integrated chips have been designed, optimized, fabricated and evaluated by the authors, which are partners in the European R&D project RAMP[1].

INTRODUCTION

Multilayer LTCC substrates offer the opportunity for low cost, high volume and small size modules for a lot of micro-wave applications since it combines the well established screen printing technique with multilayer ceramic lamination at a low firing temperature. This enables the integration of further materials to realize an increased functionality of the modules. Two drawbacks for radio frequency and power applications are the low thermal conductivity of the ceramic tape and the limitation of this technology to the lower GHz-frequency range [1]. Improved material and fabrication capabilities are now under development and are currently investigated by a European consortium in the Brite-Euram project RAMP[1]. The goal of the project is to demonstrate the capability for radio frequencies and power applications of the LTCC technology. This paper deals with optimized interconnects from waveguides in multilayer substrates to embedded chips. Two methods for feeding have been investigated: a connection with wire bonds for frequencies up to 30GHz and a coupled transition with band-pass characteristic capable for higher frequencies.

CHIP INTERCONNECT DESIGN

The aim of the design was to integrate chips in a LTCC environment. For the integration the chips have been placed on one hand in a one layer depth cavity on the topside and on the other hand in a two layer depth cavity on the backside of the LTCC. The LTCC consists of a 4 layer Ferro substrate with gold conductor on top and silver metallisation inside. Each layer has a thickness of 185 µm and a relative permittivity of 5.9.

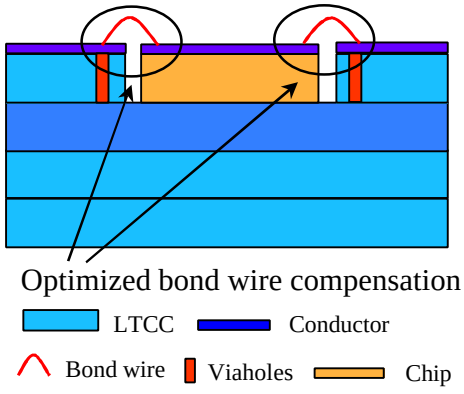

Figure 1: Side view of the microstip / coplanar chip feed.

BOND WIRE INTERCONNECT

The microstrip chip placed in the topside cavity (see Figure 1) has been designed for a microstip- and for a coplanar-environment. To enable the use of short bond wires a one layer depth cavity has been chosen for the 125 µm thick chip. For the compensation of the bond wire inductance the microstrip line width has

[1] RAMP: „Rapid Manufacture of Microwave and Power Modules", BE-97-4883

been increased at the side of the cavity (see Figure 2). The length and the width of these matching step has been optimized with 3D FDTD simulations [2]. For the field simulations the complete structure including the bond wires has been modeled. In earlier activities such interconnects have been investigated without optimization [3].

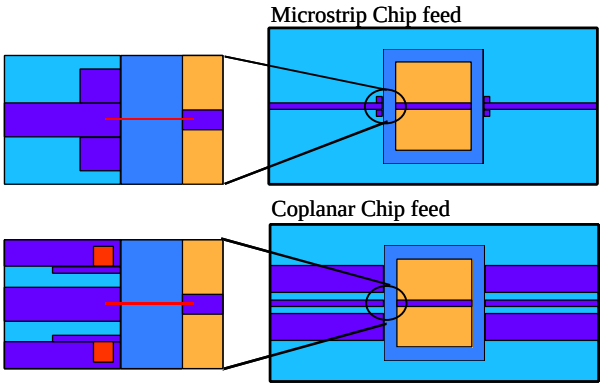

Figure 2: Top view of chip interconnects.

In case of the coplanar chip feed the bond wire has been compensated by a reduced gap width of the coplanar line at the cavity side (see Figure 2). The dimensions have been again optimized utilizing FDTD simulations. The ground plane connection is realized with two viaholes from the coplanar ground plane on the top layer to the microstrip chip ground plane.

COUPLED INTERCONNECT

The transition from the top of the LTCC to the backside cavity including the chip placement is shown in figure 3. On the top layer and in the cavity a coplanar linetype is used. The transition from the topside to the cavity has been optimized with FDTD simulations [4]. A coupling structure at the end of the coplanar line in the cavity builds the RF connection to the microstrip chip. An open ended inner conductor of the coplanar line with a reduced width achieves the coupling. The coupling structure is designed for a center frequency of 20 GHz. By changing the length of the coupling structure the frequency range of usage can be moved up or down. In the design a 3D field solver was used to be sure to include all coupling effects.

A coupled interconnect from a CPW to a microstrip line on a chip placed on top of the substrate has been investigated in [5].

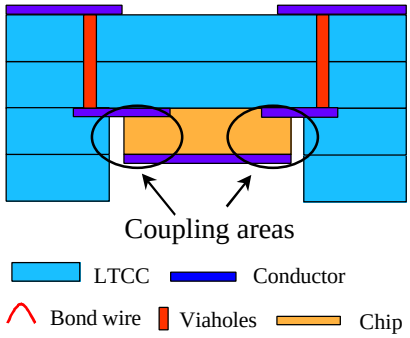

Figure 3: Cross view of the coupled chip interconnect
in the backside cavity.

PRODUCTION TOLERANCE ANALYSIS

The chip interconnects have been manufactured at Sorep-Erulec in France on a 4 layer Ferro substrate with gold metallisation on top and silver metallisation inside. In the manufacturing process the "green" dielectric tape is first cut into blanks for all layers. The vias are punched in these blanks and filled with ink. This is followed by the screen printing of the conductors on all layers. The printed blanks are collected and laminated. In the last step the laminated blanks are cofired at a temperature of about 850°. Figure 4 shows a photo of the manufactured microstrip fed (A), coplanar fed (B) and coupled interconnect (C).

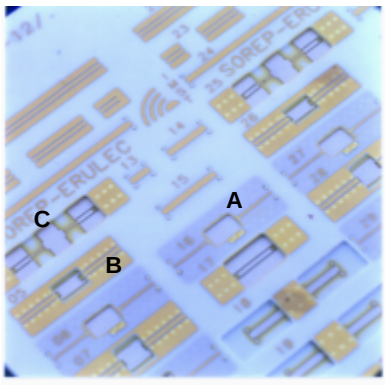

Figure 4: Photograph of LTCC tile with different interconnects and calibration lines

A tolerance analysis of the manufactured coplanar line dimensions and two large distances between two

structures on the top metallisation of the LTCC is given in Table 1. The first column specifies the part number of the different measured LTCC tiles and the first row specifies the nominal values from the layout. In the last column is the percentage shrinkage of the LTCC shown. All other entries show the difference in microns/percent from the nominal values. The total shrinkage in x- and y-direction has been determined by measuring the distances of the most upper and lower as well as the most left and right conductor edges (see table 1,2nd and 3rd column, x and y value). The deviation between the layout and the measured distance is given by Δx and Δy. The average deviation is about –0.09% in x-direction and +0.02% in y-direction, which is an excellent result. The tolerances in the realization of the coplanar line type show electrical effects. The centerline conductor of the coplanar line is processed with an average width of 380 µm (-20%) while the gap is processed with an average width of 141.5 µm (+16.5%). This leads to an impedance mismatch of about 6 Ohm. The screen-printing effects in diffuse edges of the metallisation that results in a larger effective gap width and probably in increased losses on the coplanar line. The increased effective gap width can probably be taken into account in the layouts by adding an oversize to the metallisation.

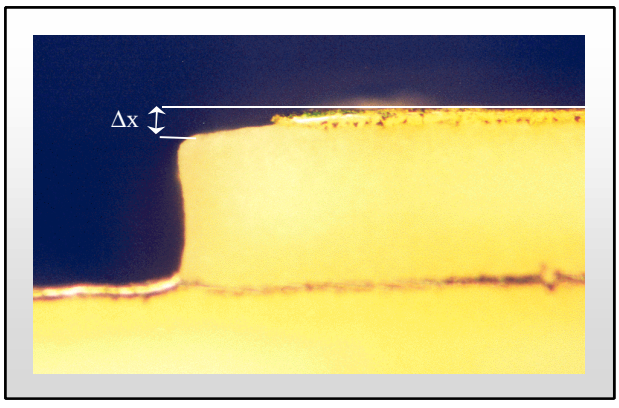

Figure 5: Cut through the LTCC at a cavity edge.

One LTCC tile has been cut into several slices to investigate the production accuracy of the cavities and the structures inside the LTCC (metallisation planes, viaholes,..). Figure 5 shows a cut through the LTCC at a cavity edge. The layer height decreased in the region of the cavity by the distance Δx. This makes it difficult to place the bond wires close to the cavity edge due to a non planar top surface. As result the bond wires must be extended and this leads to an increased parasitic inductance.

SIMULATION AND MEASUREMENTS

The comparison between simulation and measurement for the microstrip chip feed and the coplanar chip feed is shown in Figure 6. In case of the microstrip chip feed is the transmission loss for 2 interconnects below 0.5 dB up to 40 GHz while the return loss at the feeding port is better than 10 dB. Up to 28 GHz it is even better than 20 dB. Compared to the microstrip feed is the insertion loss of the coplanar chip feed (1 dB up to 30 GHz) slightly higher. This is founded in the neglection of the losses in the simulation. The matching at the feeding port is above 10 dB up to 30 GHz. The differences between simulation and measurement are caused by an impedance mismatch due to line tolerances and due to the use of longer bondwires in the chip connection.

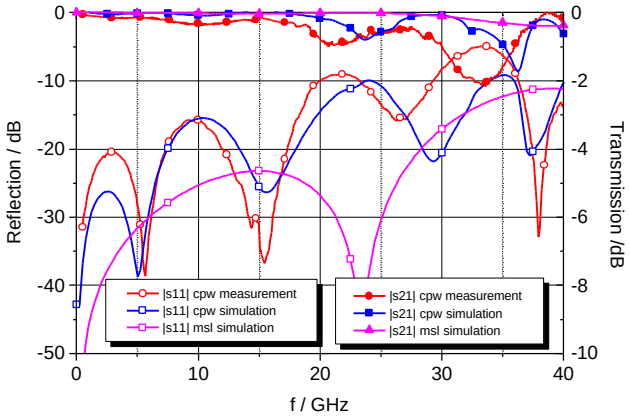

Figure 6: Simulation results of the microstip / coplanar chip feed.

Figure 7 shows the simulation and measurement results of the coupled chip interconnect. The insertion loss of the transition to the backside cavity, the double coupled chip interconnect and the transition to the top metal layer is in total 2 dB. At the feeding port a matching of 10 dB is achieved in a frequency range from 12 GHz up to 25 GHz. The differences between the insertion losses in the simulation and measurement are caused by the neglection of the

losses in the simulation. The bandwidth differs slightly between simulation and measurement due to production tolerances and due to the neglect of the conductive glue for the chip placement in the simulation.

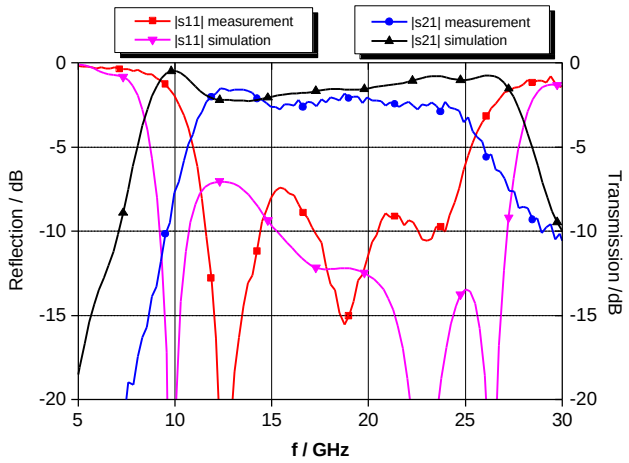

Figure 7: Simulation and measurement results of the coupled chip Interconnect.

CONCLUSION

Two different types of interconnects for LTCC´s have been presented. The designs have been done with a 3D field solver and verified by measurements. The comparison of the simulation with the measurements shows that a 3D field solver is a suitable tool to design passive multilayer structures. In the manufacturing process a good accuracy was achieved. This allows the use of LTCC´s for frequencies above 25 GHz.

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Part no	Δx / µm x=44871	Δy / µm y=46700	Δw / µm 400	Δgap l / µm gap=125	Δgap r / µm gap=125	shr / % 15
4	- 59	+ 17	-20	+23	+ 27	14.95
5	- 107	- 40	-16	+11	+ 18	15.17
6	- 46	+ 8	- 30	+ 28	+ 27	15.07
7	- 103	- 16	- 21	+ 13	+ 9	14.94
11	+ 41	+ 72	- 15	+ 13	+ 10	14.74
12	0	+ 41	- 21	+ 15	+ 15	14.86
13	- 62	- 36	- 20	+ 12	+ 16	14.98
14	- 53	+ 34	- 20	+ 22	+ 20	14.94
15	+ 30	0	- 12	+ 10	+ 9	14.88
Ø µm	- 39	+ 9	- 19.5	+ 16.3	+ 16.8	
Ø %	- 0.087	+ 0.019	- 4.9	+ 13	+ 13.4	

Table 1: Tolerance analysis of different LTCC parts.